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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,727	03/09/2004	Larry L. Byers	MP0787	1768

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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

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11/27/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,727	BYERS ET AL.	
	Examiner	**Art Unit**	
	SHANE M. THOMAS	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 48-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 48-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/2/2009 has been entered.

Response to Amendments

As per Applicant's amendments, the Examiner has cited further portions of the Gary reference as well as present the prior art of Hughes.

Applicant argues in light of the present amendments on page 14 of the present response that Gary does not teach the processors operating at different rates. The Examiner notes that while the processors P0 and P1 of Gary may be different processors [3/63-65], the Examiner agrees that Gary does not specifically disclose that the processors operate with different rates. While the Examiner maintains that such a modification would have been clearly obvious to one having ordinary skill that the rates of the processors would not have to be equal (and would be one of two possible choices - the same rates or different rates for the processors), the Examiner cites the reference of Hughes to explicitly disclose a memory system that contains a plurality of processors 1-3, where the processors generally operate in different clock rates - ¶3.

Applicant additionally argues on page 14 with regard to Gary not teaching the added limitation of the "servo controller interface being connected between the servo controller and the first and second processors" by asserting that the buffer 104 (which was interpreted by the Examiner as part of the servo controller interface) is located external to the controller 103. The Examiner respectfully disagrees with the Applicant's assessment of Gary and directs the Applicant to [33/51-54] of Gary. This citation teaches that in lieu of a buffer memory, a cache may be used in place of the buffer memory 104 by making the necessary modifications *to the memory control* 109. Thus, it could have been seen that instead of accessing an external buffer, a cache within memory control 109 could have been used instead, thereby maintaining the Examiner's position that the servo controller interface is still contained within the embedded controller comprising of every element within 103 except servo controller (combination of elements 105 and 108).

Furthermore, the Examiner presents an alternate interpretation on how Gary continues to teach the limitation of "the servo controller interface connected between the servo controller and the first and second processors." Referring to figure 2, Gary shows the processors 201 connected to the servo controller (e.g. one of the peripheral devices 202) via servo controller interface (combination of MUXes 205, busses 114, and logic 204); therefore, the servo controller interface is clearly shown as being connected between the servo controller and the processors. The servo controller interface includes speed matching module (I/O register 301, figure 3 - this register matches the speed in which the servo controller interfaces with the processors by hold read or write commands/data that are to be sent to the servo controller - [4/65 - 5/4]) and pipeline control module 204.

This interpretation of the claimed limitation shows how the Gary reference teaches, in an alternate interpretation, the newly amended claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6,48-50,52-57,59-61, and 63-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gary et al. (U.S. Patent No. 6,662,253) in view of Hughes et al. (U.S. Patent Application Publication No. 2002/0184453).

As per claims 1 and 52, Gary teaches an embedded disk controller (figure 1 sans elements 101 and 107) having a servo controller (combination of elements 105 and 108) the embedded disk controller comprising:

A servo controller interface (combination of all elements within element 103 and element of figure 1 *except* servo controller (elements 105 and 108)) that includes a speed-matching module (cache used in place of a buffer memory - [3/48-54] and a pipeline control module (MUX set 205 and logic 204 shown in figures 2 and 3) such that at least two processors (P0 110 and P1 111), which are being considered to be first and second processors, share memory mapped registers without conflicts [4/65 - 5/13] and [5/29-49]. Gary teaches in section [4/65 - 5/13] that peripheral devices are shared among the processors P1 and P0, wherein each device is memory mapped to a designated address space, and wherein that range of memory mapped

addresses includes identification for registers. Therefore, it can be see that because the processors share the peripheral devices without conflict and each device has its own registers that are memory-mapped, that the processors share the memory mapped registers without conflicts. The pipeline control module 205 serializes access to the devices to one processor at a time as discussed in [5/29-49].

Gary goes on to teach that the servo controller interface is connected between the servo controller and the first and second processors (as shown in figure 1, the servo controller interface is connected between the processors and the servo controller by means of the MUX portion 205 of the servo controller interface as defined above by the Examiner.

Gary teaches that the processors may be different [3/63-65] but does not specifically teach wherein the first and second processors operate at different rates. Hughes teaches a memory system where processors generally operate at different clock rates (¶3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the servo controller system of Gary with the teaching of processor cores operating at different clock cycles as taught by Hughes in order to have achieved the predictable result of the processors P0 and P1 of Gary being capable of operating at different rates.

As an alternate interpretation of claim 1, please refer to the discussion in the "Response to Amendments" section above.

As per claims 2,53,64,72, and 80, Gary teaches in [3/63-65] that the processors P0 and P1 may be different to optimize particular tasks. As taught above, Hughes teaches different processors within the same system operating at different clock rates. It would have been obvious

to one having ordinary skill in the art to have used different processor frequencies to optimize the desired performance for the specific desired tasks.

As per claims 3 and 54, it is necessarily inherent that the bus element connecting the servo controller interface (defined supra) to the servo controller (also defined supra) operates at a given frequency. As such, claims 3 and 16 are anticipated since the claim only states that the servo controller and the servo controller interface must operate in the same or different frequency domains. Since the controller and the interface are in operation together (as the disk controller 103 of Gary can used to access a disk medium 107) it is necessarily inherent that they are operating either in the same frequency domain or different frequency domains.

As per claims 4,55,68,76, Gary teaches [3/45-51] that the speed matching module 104 ensures communication between the host and the disk controller 103 without inserting wait states to the servo controller interface when writing to the servo controller. In other words, because of the difference in frequency domains in which the disk drive and host operate, all incoming write data is buffered in the speed-matching module 104 before being written to the hard drive 107. The write can then be supplied to the disk drive 107 via the servo controller (105+108) from the servo controller interface (defined supra) without the servo controller interface inserting wait states (between write data). Essentially (as known in the art) the speed-matching module allows the servo controller to find the location of the data that is to be written and then supplies the data to the servo interface to be written to the disk drive. This process repeats with the speed-matching module reading the data for next location of data to be written while the servo controller reads the disk drive to that data location. Then once the location has been accessed, the data is supplied from the interface to the controller (105+108); thereby preventing wait states

or having the servo controller interface *itself* wait for the data from the host 101 while the controller rotates the disc heads to the proper location on the disk.

As per claims 5 and 56, according to Gary, because of the pipeline control module 205, the processors exclusively share access to the disk drive 107 [6/55-67], and a situation cannot arise where both processors are reading from the disk drive at the same time (i.e. read conflict).

As per claims 6 and 57, the pipeline control module 205 comprises a hardware mechanism for indivisible register access [7/7-15] to the first or second processor. In other words, only one processor may be the owner of the peripheral's I/O register 301 (figure 1), thereby being able to access the peripheral [5/23-27].

As per claims 48,59,69,77, and 84 the pipeline control module 205 resolves conflict (simultaneous access request from both processors for the same resource) between the first and second processor transactions (for access control) [6/48-54] - the protocol logic 204 of the pipeline control module 205 (figure 1) implements the dynamic sharing of the peripherals with the processors.

As per claims 49 and 60, as shown in figure 1, the first and second processor communicate with the servo controller via separate buses (both labeled 102) - [4/2-3].

As per claims 50 and 61, assuming processor P1 is the owner of a given peripheral (in this case the disk drive 107 itself), the pipeline control module 205 will hold write access to the second processor P0 until the first processor releases the peripheral from its ownership - [6/55 - 7/6].

As per claims 63,71, and 79, Gary teaches a disk controller 103 having servo controller (combination of elements 105 and 108), the servo controller interface (combination of all elements within 103 except 105 and 108) comprising:

a first interface (connection between processor 110 and bus 102) for communicating with a first processor 110 over a first bus 102 (figure 1) at a first rate (rate at which the processor is operating) and a second interface (connection between processor 111 and bus 102) for communicating with a second processor 111 over a second bus 102 (figure 1) at a second rate (rate at which the second processor is operating). Since bus 102 is separated by a MUX 205, the Examiner is considering each bus connecting a respective processor 110,111 to be a separate bus despite identical numbering. Gary further teaches the servo controller interface (e.g. combination of all elements within element 103 of figure 1 *except* servo controller (elements 105 and 108)) selectively granting one of the first and second processors access to a servo controller (whichever processor supplies the “owner” signal - [4/37-40] and [5/28-49].

Gary does not specifically teach but Hughes teaches wherein the clock rates of the processors are different. Hughes teaches a memory system where processors generally operate at different clock rates (¶3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the servo controller system of Gary with the teaching of processor cores operating at different clock cycles as taught by Hughes in order to have achieved the predictable result of the processors P0 and P1 of Gary being capable of operating at different rates.

As an alternate interpretation the claim, please refer to the discussion in the "Response to Amendments" section above.

As per claims 65,73, and 81, Gary teaches a speed matching module 109 (e.g. cache within memory control 109 that can be used in place of buffer memory 104) resolves conflicts between at least a first (host) and second (disk) clock domains [3/45-58].

As per claims 66,74, and 82, Gary teaches the speed matching module 109 transitions servo controller accesses (via buffering in cache that performs the functions of buffer 104 as taught in [3/45-58]) from one of the first (host) and second clock domains (disk) to the other first and second clock domains [3/45-51]. As known in the art, a buffering element from one frequency domain writes data to a buffer while the element in the second frequency domain reads the data, thereby resolving the differences between the first and second domains.

As per claims 67,75, and 83, it can be seen that the memory mapped registers are within the servo controller (105 and 108) since Gary teaches that each peripheral device attached to the MUX 205 has a peripheral register [4/65 - 5/2] that buffers data going to and coming from those peripherals. It can therefore be seen that since the servo controller is attached to the peripheral, the memory mapped registers may be within the servo controller.

As per claims 70,78, and 85, the servo controller interface, by means of the pipeline control module 205, delays a write access for one of the processors 110,111 during write conflicts. Assuming processor P1 is the owner of a given peripheral (in this case the disk drive 107 itself), the pipeline control module 205 will hold write access to the second processor P0 until the first processor releases the peripheral from its ownership - [6/55 - 7/6], thereby overcoming write conflicts.

Claims 7,51,58, and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gary et al. (U.S. Patent No. 6,662,253) in view of Hughes et al. (U.S. Patent Application Publication No. 2002/0184453), as applied to claims 6 and 57 above, in further view of Snyder et al. (U.S. Patent No. 6,745,274).

As per claims 7,51,58, and 62, Gary suggests the need for a processor that loses a race condition when vying for a common resource to be made aware that it failed to acquire the resource (to be able to reschedule the write data in one example presented by Gary) but does not specifically teach using a semaphore to control sharing access of the common resource. Snyder teaches a semaphore to synchronize access to a shared resource [1/22-25] and [2/26-38] without requiring special instructions to implement the synchronization control [8/31-36]. Further, Snyder teaches in [4/37-40] that the use of the semaphore allows for processor that did not successfully acquire the shared resource to "learn of the failure" and re-attempt to acquire the semaphore lock - thereby providing a resolution to the suggestion of Gary - [7/11-15].

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the disk controller system of Gary with the teaching of a semaphore of Snyder in order to have implemented a sharing technique that would have allowed a processor (p0, p1) of the system of Gary to have determined that it lost or did not acquire a shared resource when both processors simultaneously request access to the shared peripheral. Once the determination is made, the losing processor may vie for the semaphore lock again to access the peripheral once the other processor releases the lock (figure 2, step 200 of Snyder).

Further regarding claims 51 and 62, Snyder teaches that the hardware mechanism of the disk controller system of modified Gary can be a semaphore register [2/20-21].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ward et al. (U.S. Patent Application Publication No. 2004/0221133) teaches (¶8) a bus system for use between two processors within the same system operating at different clock speeds.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHANE M. THOMAS whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Shane M Thomas/
Primary Examiner, Art Unit 2186